Bridged-Grain Solid-Phase-Crystallized Polycrystalline-Silicon Thin-Film Transistors

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***Abstract*—Novel bridged-grain (BG) technique is applied in the fabrication of low-temperature solid-phase-crystallized polycrystalline-silicon thin-film transistors. As a result of improved current flow and reduction of high drain electric field, the subthreshold slope, threshold voltage, maximum field-effect mobility, leakage current, and on–off ratio are greatly improved. Mechanisms of BG conduction are studied in detail.**

***Index Terms*—Bridged grain (BG), polycrystalline silicon (poly-Si), thin-film transistors (TFTs).**

I. Introduction

LOW-TEMPERATURE polycrystalline-silicon (poly-Si) (LTPS) technology is one of the most promising technologies to produce high-performance thin-film transistors (TFTs) for both applications to pixel switching and peripheral circuits in flat-panel display backplanes [1]. Among all LTPS technologies, solid-phase crystallization is the simplest and most direct method to get poly-Si thin films with high uniformity and low cost [2]. The main drawbacks of solid-phase crystallization technology are small grain size and high density of grain boundaries (GBs) inside the poly-Si film [3]. High density of GBs results in high threshold voltage (V_{th}), poor subthreshold slope (SS), and low carrier mobility in solid-phase-crystallized (SPC) poly-Si TFT [4], which seriously limit its application in driving circuits of active matrix displays. Several methods have been proposed to reduce GBs, including high-temperature postannealing [5], [6] and plasma passivation [7]–[9]. However, both methods have critical drawbacks. For high-temperature postannealing, the temperature is often above 900 °C, which prevents its application to low-cost glass substrates. For plasma passivation, additional issues such as sensitive device performance due to process variation [8] and reliability problems emerge [10].

In this letter, a new device named bridged-grain (BG) poly-Si TFT is proposed. Instead of enlarging the grain size during the crystallization process, the idea of BG technology aims to build bridges to link the small grains. The bridges between the grains are formed by doping the channel with heavily doped bridge lines perpendicular to the active channel. As a result, a series of short channels is formed. SPC TFT with BG structure shows great improvements in terms of V_{th}, on–off ratio, SS, maximum field-effect mobility (μ_{FE}), and gate-induced drain leakage (GIDL). At the same time, the thermal budget of crystallization remains unchanged.

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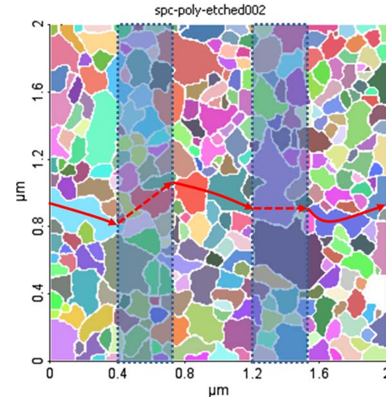

Fig. 1. Schematics of current flow in BG poly-Si based on grain detection results.

II. Conduction Mechanism of BG

To understand the mechanism of BG conduction, the crystallization quality of SPC poly-Si film is first characterized. An atomic force microscope (AFM) is applied to confirm the grain size through examining the surface topography of the SPC poly-Si film after tetramethylammonium hydroxide etching. With the help of the AFM watershed grain detection program [11], it was found that the mean value of the grain size is about 150 nm, as shown in Fig. 1. The existence of such small grains and the high density of GBs are the main causes of poor SS, high leakage current, and high V_{th} of SPC TFTs [4].

The principle of improved current flow in SPC poly-Si with BG structure is schematically shown in Fig. 1. Submicrometer-scale heavily doped regions are represented as the blue regions enclosed by the dashed lines. These doped regions are the BG lines. The channel is divided into several segments and bridged by the BG lines. The red lines with arrows represent a possible path of current flow. In every segment of the channel, larger current goes into the more conductive path with less GBs. These paths are not straight lines and are dependent on the grain size, shape, and grain distribution. When the carriers enter the conductive BG regions, they can flow freely in all directions. The carriers will pick up the most direct path (shown with red dashed lines) which leads to the path with less GBs in the next segment of the channel. The BG regions therefore provide shortcuts to the carriers and help the carriers to find the more conductive path. Consequently, the number of barriers

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and traps along the current path is greatly reduced, which would directly result in lower V_{th} and SS, higher mobility, and smaller thermal leakage current $I_{\min}$. The improvements are expected to be maximum when the length of the channel segment is comparable to the grain size.

In addition to the improvement of current flow, the BG lines also serve for electric field averaging. It is well known that, when the TFT is turned off, high electric field exists at the reverse-biased drain junction. The leakage current increases exponentially as a function of this reverse electric field [12], [13]. Moreover, high drain electric field seriously affects the long-term reliability of the TFT. Several drain electric field relief structures have been proposed in the past, among which the lightly doped drain (LDD) structure [14] and split-gate design [15] are most extensively studied. However, the LDD structure suffers from large ON-state resistance and results in small ON-state current. On the other hand, due to the design rule of large-area TFT panel, scaling down the devices to submicrometer scale on large area with precise alignment and good exposure quality cannot be realized at present. Therefore, for split-gate design, the area for one TFT will be greatly enlarged when the number of split gates increased. For BG SPC TFT, a large number of submicrometer-scale reverse-biased junctions are formed in the channel at the OFF state. It is similar to the split-gate case. The peak electric field near the drain is partially distributed to the edge of the BG lines, resulting in reduced electric field and lower GIDL. With increasing number of BG lines inside the channel, the electric field and GIDL can be further reduced. These submicrometer-scale BG lines can be uniformly patterned using laser interference photolithography or nanoimprinting technology. With advances in nanoprinting technology, it is possible to produce fine patterns over large area [16]. This provides a promising way to realize BG in large-scale production. No photomask or precise alignment to other masks is required. The area of one TFT is the same as that of the conventional single-gate design. The detailed fabrication process is described in Section III.

III. Device Fabrication

The fabrication process began with 4-in silicon wafers covered with 500-nm thermal oxide. One-hundred-nanometer amorphous silicon was deposited by low-pressure chemical vapor deposition (LPCVD) as active layer. Solid-phase crystallization process was then carried out through annealing at 600 °C for 24 h in N_2 ambient. After crystallization, antireflection coatings (ARCs) and photoresist were spin coated. The photoresist was then patterned into gratings with a period of 800 nm through laser interference lithography. The setup of the lithography system is in the form of a Lloyd mirror interferometer [17]. Structures of the patterned photoresist are captured by a scanning electron microscope (SEM) and shown in Fig. 2(a). The length ratio of the photoresist-covered region and the exposed region in one period is about 2:1. Boron ions were then implanted into the exposed areas of the SPC film. The implantation dose and energy were $2 \times 10^{15}/\text{cm}^2$ and 23 keV, respectively. After implantation, the photoresist and ARC layer were removed, and the BG lines were formed. There was no annealing added at this step to activate the dopants for BG. The grain size of the SPC film remains the same. The SPC poly-Si layer was then patterned into active islands. Seventy-

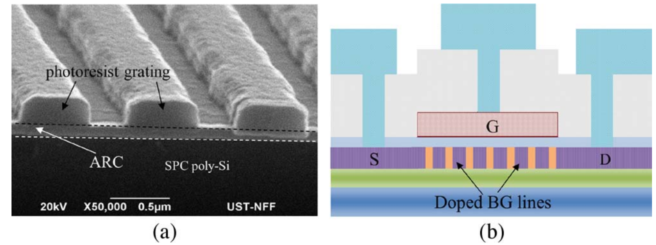

Fig. 2. (a) SEM picture of photoresist grating and (b) schematics of device structure (cross section).

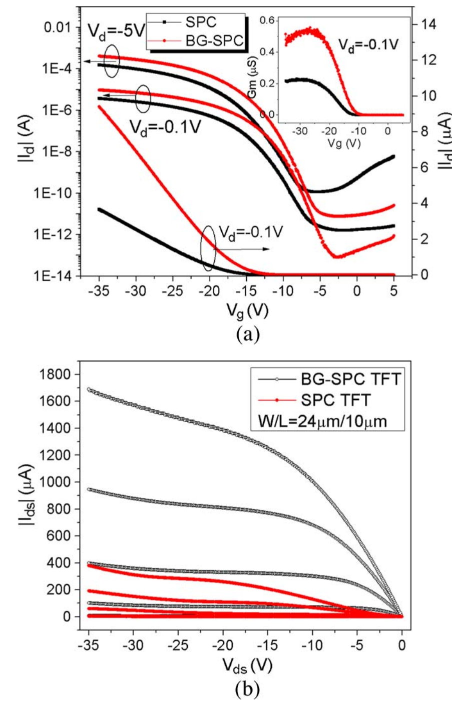

Fig. 3. Comparison of (a) transfer characteristics and (b) output characteristics of conventional SPC/BG SPC TFTs ($W/L = 24\ \mu\text{m}/10\ \mu\text{m}$).

nanometer SiO_2 was deposited by LPCVD at 425 °C as gate dielectric. Then, 200-nm Ti was sputtered and patterned as gate electrode. Self-aligned 33-keV boron implantation was done at the dosage of $4 \times 10^{15}/\text{cm}^2$. Five-hundred-nanometer LPCVD SiO_2 was deposited, and contact holes were defined. Seven-hundred-nanometer Al–1% Si was sputtered and patterned as testing pads. The devices were then sintered in forming gas for 30 min at 420 °C.

The dopants for source/drain and BG regions are activated simultaneously during the SiO_2 deposition and forming gas annealing process. The schematic of the structure of the BG SPC TFT is shown in Fig. 2(b). n-type BG SPC TFTs can also be made if the dopant for BG and source/drain is changed to phosphorus. Measurements of device characteristics were done using an HP4156B semiconductor parameter analyzer. Channel lengths (L) for SPC and BG SPC devices are 10 and $10 \times 2/3\ \mu$m, respectively, with a channel width (W) of 24 μm.

IV. Results and Discussion

The transfer characteristics of conventional SPC TFT and BG SPC TFTs measured at $V_{\text{ds}} = -0.1$ and -5 V are shown in Fig. 3(a).

TABLE I
PARAMETER EXTRACTION OF SPC/BG SPC TFTs

	SPC	*BG-SPC*	*Definition*
V_{th}(V)	-13.8	-11.7	V_g when $\|I_d\|$ reached $W/L \times 10^{-7}$A at $V_d = -5$V
SS(V/dec)	1.68	1.35	Slope of the log| Id| in 10^{-10}A range at $V_d = -5$V
I_{min}(A)	1.14×10^{-10}	7.53×10^{-12}	Minimum I_d at $V_d = -5$V
I_{max}(A)	1.53×10^{-4}	4.06×10^{-4}	Maximum I_d at $V_d = -5$V
on-off Ratio	1.34×10^{6}	5.39×10^{7}	I_{max} / I_{min}
G_m(S)	2.29×10^{-7}	5.58×10^{-7}	Transconductance at $V_d = -0.1$ V
μ_{FE}(cm²/Vs)	19.3	30.7	$\mu_{FE} = \frac{LG_m}{WC_{ox}V_{ds}}$ $C_{ox} = 4.93\times10^{-4}\, F\cdot m^{-2}$
GIDL(pA/μm)	613	2.58	I_d at $V_g = 5$ V and $V_{ds} = -5$ V, divided by W

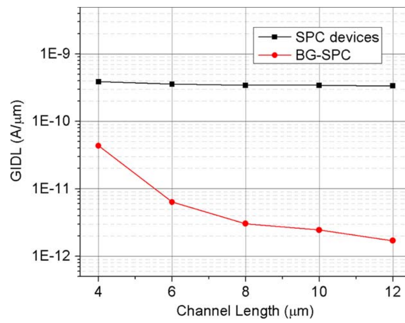

Fig. 4. GIDL of SPC/BG SPC TFTs with different L's.

The inset of Fig. 3(a) shows the G_m measured at $V_{\rm ds} = -0.1$ V. Compared with conventional SPC devices, all important parameters, including the $V_{\rm th}$, SS, on–off ratio, field-effect mobility, and leakage current, are greatly improved as expected. The $V_{\rm th}$ is lowered by 2.1 V. SS is reduced by 330 mV/decade. The field-effect mobility estimated from the transconductance is improved by 59%. The channel length used for BG SPC TFT is $10 \times 2/3$ μm for calculation of $\mu_{\rm FE}$ and $V_{\rm th}$. A comparison of key parameters of SPC and BG SPC devices is listed in Table I. It can be seen that $I_{\max}$ is boosted by 2.65 times. This value is much larger than the value estimated due to channel length modification (1.5 times). It is due to the improvement of both carrier mobility and reduction of $V_{\rm th}$ by the BG lines. The output characteristics of these two types of TFTs are shown in Fig. 3(b). The curves are measured at $V_{\rm gs} = -10$, -15, -20, -25, and -30 V. The saturation current is enhanced by more than four times without any kink effect at very high drain voltage. As the saturation current is proportional to $(V_{\rm gs} - V_{\rm th})^2$, more enhancement of saturation current than the linear current is observed, which is linearly proportional to $(V_{\rm gs} - V_{\rm th})$.

The most noticeable improvement is the suppression of leakage current. GIDL current is governed by the field-enhanced tunneling. The holes in the conduction band are assisted by the electric field to tunnel toward the valence band via GB traps, whereas the leakage current $I_{\min}$ is mainly induced by the thermally generated carriers via trap states [18]. Compared with that of SPC devices, GIDL of BG SPC devices is suppressed by more than 230 times. $I_{\min}$ is decreased by 15 times. With increasing number of BG lines inside the channel, the electric field, and therefore GIDL, is further reduced, as shown in Fig. 4.

V. CONCLUSION

A novel device named BG SPC TFT has been demonstrated. The results show great improvements in on/off-current ratio, $V_{\rm th}$, SS, and GIDL. These improvements are attributed to the application of submicrometer-scale BG structures to provide shortcuts to improve the current flow and reduction of the drain electric field. These improvements of BG SPC TFT make it a promising candidate for the realization of peripheral circuits for high-aperture-ratio active matrix displays at low cost. Indeed, BG technique enables a low-cost LTPS technology such as solid-phase crystallization to compete with more advanced technologies such as excimer laser annealing.

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